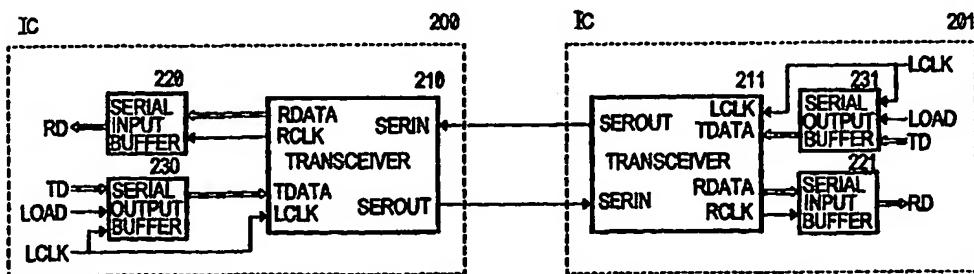




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G06F 13/42, G11C 5/06	A1	(11) International Publication Number: WO 98/45787 (43) International Publication Date: 15 October 1998 (15.10.98)
(21) International Application Number: PCT/US97/21936 (22) International Filing Date: 25 November 1997 (25.11.97) (30) Priority Data: 08/838,813 10 April 1997 (10.04.97) US (71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US). (72) Inventor: BELL, Russell; 7102 Beauford Drive, Austin, TX 78750 (US). (74) Agent: ZAHRT, William, D., II; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).		(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>

(54) Title: PIN COUNT REDUCTION THROUGH SERIALIZATION TECHNIQUES



(57) Abstract

A method and circuit for reducing the pin count of semiconductor devices through high-speed serialization technique. Normally parallel data is bundled into a serial data package, serialized, and sent through a single pin. At the receiving semiconductor device, the serial data package is received through a single pin and deserialized.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakhstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

PIN COUNT REDUCTION THROUGH SERIALIZATION TECHNIQUES

Technical Field

The invention relates generally to semiconductor devices having inter-device connections and more particularly to reducing pin count in such devices.

5 Background Art

Modern semiconductor devices, or "chips," form their electrical connections with the outside world through pins. Pins used for a variety of purposes such as applying power and ground reference potentials to chip and carrying signals
10 consume space on the chip and often require expensive packages; thus it is generally desirable to minimize the number of pins.

Another purpose for pins is to provide electrical connections for transferring bit data from one chip to another chip. Conventional chips use multiple pins to input and output
15 multiple-bit data. For example, in Fig. 1(a), conventional IC 110 transmits eight-bit parallel data to IC 120 using transmit data pins TD0 - TD7 and a transmit data strobe pin TDS. The strobe pin TDS is used for signaling that the multiple-bit data on pins TD0 - TD7 is valid. IC 120 receives the eight-bit byte
20 at pins RD0 - RD7, when signalled by receive data strobe RDS. Thus, transmitting and receiving an eight-bit byte require eighteen pins on each chip in a conventional design.

Other conventional chips use a set of bi-directional pins to transmit and receive parallel bit data. In Fig. 1(b),
25 IC 111 transmits an eight-bit byte to IC 121 using bi-directional pins D0 - D7 in addition to strobe pins TDS and TRS. In this configuration, the number of pins required is ten.

Switching multiple pins on the parallel bus from high
30 to low, however, produces a significant amount of current sinking that must pass through the package ground and I/O pins, which results in a significant amount of ground bounce and electromagnetic interference ("EMI").

The ground bounce is a voltage spike caused by the lead frame/pin inductance and is directly proportional to $L \frac{di}{dt}$; where $\frac{di}{dt}$ is the change in the aggregate current per unit of time caused by the switching of all the pins. Thus, the voltage spikes become worse as the system clock rate increases and as more parallel bits are switched. Ground bounce is a problem because voltage spikes can cause internal chip elements to fail. EMI is also a concern because it creates noisy signals, causing the device to misoperate.

Therefore, a need exists to reduce the pin count of semiconductor devices and to curb the electrical problems of ground bounce and EMI associated with switching multiple pins simultaneously.

Disclosure of the Invention

A principal objective of the present invention is to provide a method for transmitting a multiple bit signal between two chips that uses fewer pins than conventional technology. A further objective of the invention is to provide a method for transmitting a multiple bit signal between two chips that reduces the amount of ground bounce and EMI.

According to the present invention, the foregoing and other objects and advantages are attained by a circuit for converting parallel bits into a bit stream comprising a serial output buffer and a digital, high-speed transceiver. The serial output buffer receives the parallel bits and outputs a nybble stream to the transceiver. The transceiver receives the nybble stream and encodes the nybbles into the bit stream. In another aspect, the serial output buffer concatenates addressing information to the parallel bits.

In accordance with one embodiment of the invention, a circuit for converting a bit stream into parallel bits comprises a digital, high-speed transceiver and a serial input buffer. The transceiver receives the bit stream and decodes the bit stream into a nybble stream and a recovered clock signal. The serial input buffer receives the nybble stream and the recovered clock signal and outputs the parallel bits based upon the nybble stream and the recovered clock signal. Preferably, the serial input buffer outputs the parallel bits

in response to addressing information embedded in the bit stream.

In accordance with another aspect of the invention, provided is a method for transmitting a data bits from a source semiconductor device to a target semiconductor device. The source semiconductor device serializes the data bits into a bit stream and outputs the bit stream through a single pin of the device. The target semiconductor device receives the bit stream through a single one of its pins. Finally, the target semiconductor device deserializes the bit stream into the data bits. Preferably, addressing information is added to each serial data package to identify the target semiconductor device.

Brief Description of the Drawings

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Figs. 1(a) and 1(b) are block diagrams of a connection between two conventional semiconductor devices.

Fig. 2 is a block diagram showing connections between two semiconductor devices according to the present invention.

Fig. 3(a) is a block diagram showing a high-speed, all-digital transceiver implemented in the invention.

Fig. 3(b) is a timing diagram of the signals of the high-speed all-digital transceiver of Fig. 3(a).

Figs. 4(a) and 4(b) are block diagrams showing an embodiment of a serial output circuit in accordance with the invention.

Figs. 5(a) and 5(b) are block diagrams showing an embodiment of a serial input buffer in accordance with the invention.

Best Mode for Carrying out the Invention

A circuit and method for reducing the pin count of an integrated circuit are described. In the following description, for the purposes of explanation, numerous specific

details are set forth to provide a thorough understanding of the present invention. It will be apparent, however, that the present invention may be practiced without these specific details. In other instances, well-known structures and devices
5 are shown in block diagram form to avoid unnecessarily obscuring the present invention.

With reference to Fig. 2, provided is a serial link connection, using minimal switching, between IC 200 and IC 201, allowing serial information to represent the normally parallel
10 data that are provided by multiple pins. The parallel bus structure is replaced by a serial link that places data bits **TD** into a serial format.

IC 200 comprises transceiver 210 and serial output buffer 230; IC 201 comprises transceiver 211 and serial input
15 buffer 221. ~~IC 200 sends parallel data TD~~ to IC 201 by latching parallel data **TD** into serial output buffer 230 with load signal **LOAD**. Serial output buffer 230 packages parallel data **TD** into data package **TDATA** and clocks it out to transceiver 210 using local clock **LCLK**.

20 As described in more detail below, transceiver 210 serializes data package **TDATA** using local clock **LCLK** into a serial data stream, output at pin **SEROUT**. Pin **SEROUT** of IC 200 is coupled to pin **SERIN** of IC 201, where transceiver 211 receives the serial data stream and deserializes it into data
25 package **RDATA** and recovered clock **RCLK**.

Serial input buffer 221 receives data package **RDATA** and recovered clock **RCLK** and transforms them into parallel bit data **RD**.

Both transceivers 210 and 211 are described with
30 reference to transceiver 300 of Fig. 3(b). A preferred embodiment of the invention uses for transceiver 300 a high-speed, all-digital serializer and deserializer, described in U.S. Patent No. 5,400,370 issued to Guo on Mar. 21, 1995, incorporated herein by reference. Transceiver 300 is all-
35 digital, in that it does not implement large, lumped, analog components, such as capacitors, for data storage, timing, or other functions and hence be readily implemented in large scale integrated circuitry.

Transceiver 300 has three major components, deserializer 310, digital phase adjustment circuit 320, and serializer 330. Serializer 330, described in U.S. Patent No. 5,349,612, issued to Guo et al. on September 20, 1994, incorporated herein by reference, receives parallel data package **TDATA**, in N-bit nybbles clocked by local clock **LCLK**. The operation of serializer 330 in serializing an N-bit nybble **TDATA** is described with reference to the timing diagram in Fig. 3(b).

For each cycle of local clock **LCLK**, serializer 330 generates N cycles of bit clock **BCLK**, the first bit clock cycle being aligned with an edge of local clock **LCLK**. The period of bit clock **BCLK** is at most the period of local clock **LCLK** divided by N; the bit clock period does not have to be an integral fraction of the local clock period. The cycles of bit clock **BCLK** are produced by a cascade of adjustable, digital delay elements, which are preferably calibrated by an on-chip digital servo subcomponent of serializer 330, described in U.S. Patent No. 5,457,719, issued to Guo et al. on October 10, 1995. The result of the calibration circuit is sent as signal **ADJ** from serializer 330 to also calibrate the adjustable, digital delay elements of digital phase adjustment circuit 320.

Given parallel data nybble **TDATA** and generated bit clock **BCLK**, serializer 330 encodes nybble **TDATA** into a bit stream **SEROUT**, which may be an ECL signal for high-speed transmission. One encoding, as shown in Fig. 3(b) is NRZI (Non-Return to Zero, Invert on one), where a transition signifies a one and a lack of a transition signifies a zero. Other encodings such as NRZ or Manchester may be used as well.

When transceiver 300 receives an incoming serial data stream **SERIN**, the clock signal for incoming serial data stream **SERIN** is generally out of phase with respect to bit clock **BCLK**. Therefore, digital phase adjustment circuit 320 shifts the phase of the bit clock **BCLK** to create shifted bit clock **SBCLK**, having a timing edge aligned with the center of the data eye of the incoming serial data stream **SERIN**. Deserializer 310 takes shifted bit clock **SBCLK** and decodes incoming serial data stream **SERIN** into received data nybble **RDATA**. Deserializer 310 is described in more detail in U.S. Patent No. 5,367,542,

issued to Guo on November 22, 1994, incorporated herein by reference.

According to one embodiment of the invention, serial output buffer 230 is implemented by serial output shift register 410 and transceiver 400, shown in Fig. 4(a). Serial output shift register 410 receives parallel bit data **TD** and shifts out a series of N-bit nybbles **TDATA** in response to load signal **LOAD** using local clock **LCLK**. Upon each cycle of local clock **LCLK**, N-bit nybble **TDATA** is serialized by transceiver 400 and sent out through a single pin.

In Fig. 5(a), transceiver 500 receives serial data stream **SERIN** through a single pin and recovers each N-bit nybble **RDATA** and recovered clock **RCLK**. Using recovered clock **RCLK**, each N-bit nybble **RDATA** is shifted into serial input shift register 520. Serial input shift register outputs parallel data **DATA** to latch 550. Also receiving recovered clock **RCLK** is counter 530 which counts the total number of nybbles for the serial data package, and outputs the result to match logic 540. When the correct count of nybbles is received, match logic 540 output transfer signal **XFER** to latch 550. Upon receiving transfer signal **XFER**, latch 550 will latch parallel data **DATA** so that received parallel bit data **RD** becomes available to the rest of the chip.

Hence, what was parallel data at one chip is converted to a serial format, transmitted serially to another chip, recovered, and converted back to parallel data, effectively eliminating the requirement for the parallel bus. Therefore, only two pins are required to send and receive a plurality of bits, whereas, for example, nine pins are required by conventional technology to send eight bits in parallel. Accordingly, since only one pin on each chip is being switched, the ground bounce and other undesirable electrical effects associated with switching multiple pins simultaneously are eliminated. Finally, the use of a high-speed serializer and deserializer that encodes and recovers a faster clock signal ensures comparable performance.

In another embodiment of the invention, referring to Fig. 4(b), additional information, including destination address **DEST ADDR**, is concatenated to transmit data **TD** to

create a data package. Destination address **DEST ADDR** indicates which chip is to receive the data package. In Fig. 5(b), serial input buffer **521** receives deserialized data package **RDATA**, decodes an embedded address, and outputs it as received address **ADDR**. Match logic **541** compares received address **ADDR** to the address of the chip. Only if the two addresses match and counter **531** has reached the correct value, match logic **541** signals latch **551** with transfer signal **XFER** to latch parallel data **DATA**.

10 In this manner, a chip directs a data package to a specific chip, even though there are other chips attached to the same 1-bit bus.

15 In this disclosure there is shown and described only the preferred embodiment of the invention, but, as aforementioned, it is to be understood that the invention is capable of use in various other combinations and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein.

CLAIMS

1. A serial output circuit for converting a plurality of bits into a bit stream, comprising:

a serial output buffer for receiving a load signal, a local clock signal and said plurality of bits and for
5 outputting a nybble stream containing said plurality of bits; and

a digital, high-speed transceiver, coupled to said serial output buffer, for receiving the nybble stream and the local clock signal and for encoding the nybble stream with the
10 local clock signal as said bit stream.

2. The circuit of claim 1, wherein:

said serial output buffer is configured to concatenate a destination address to the plurality of bits and output a nybble stream containing said plurality of bits and the
5 destination address.

3. A serial input circuit for converting a bit stream into a plurality of bits, comprising:

a digital, high-speed transceiver for receiving said bit stream and for generating a recovered nybble stream and a
5 recovered clock signal based on said bit stream; and

a serial input buffer, coupled to said digital, high-speed transceiver, for receiving the recovered nybble stream and the recovered clock signal and for outputting said plurality of bits based on the recovered nybble stream and the
10 recovered clock signal.

4. The circuit of claim 3, wherein said serial input buffer comprises:

a serial input shift register, coupled to said transceiver, for shifting the recovered nybble stream with the
5 recovered clock signal, and for outputting a received plurality of bits based upon the nybble stream;

a counter, coupled to said transceiver, for counting the cycles of the recovered clock signal and for outputting a clock signal count;

10 match logic, coupled to said counter, for receiving the clock signal count and generating a transfer signal based upon the clock signal count; and

a latch, coupled to said serial input shift register and said match logic, for latching the received plurality of
15 bits in response to the transfer signal and outputting said plurality of bits.

5. The circuit of claim 4, wherein:

said serial input shift register is configured to output a destination address based upon the nybble stream; and

said match logic is coupled to said serial input shift
5 register and is configured to generate the transfer signal based upon the clock signal count and the destination address.

6. The circuit of claim 5, wherein:

said match logic is configured to compare the destination address with a chip address and generate the transfer signal based upon the clock signal count based upon
5 the comparison of the destination address and the chip address.

7. A method for transmitting a plurality of data bits from a source semiconductor device to a target semiconductor device, comprising the steps of:

serializing said plurality of data bits into a serial
5 data package with a first digital, high-speed transceiver at said source semiconductor device;

outputting said serial data package through a single pin of said source semiconductor device;

transmitting the serial data package from said signal
10 pin of said source semiconductor device to a single pin of said target semiconductor device;

receiving said serial data package through the single pin of the target semiconductor device; and

deserializing said serial data package from the single
15 pin of said target semiconductor device into said plurality of

bits with a second digital, high-speed transceiver at said target semiconductor device.

8. The method of claim 7,

wherein the step of serializing said plurality of data bits into a serial package with a digital, high-speed transceiver at said source semiconductor device, comprises the

5 steps of:

concatenating said plurality of data bits with an address signal into a data package, and

serializing the data package into said serial data package with the digital, high-speed transceiver; and

10 wherein the step of deserializing said serial data package into said plurality of bits with a digital, high-speed transceiver at said target semiconductor device, comprises the steps of:

15 deserializing the amplified serial data package with a digital, high-speed transceiver into a stream of serial bits, a recovered clock, and a decoded address signal,

latching the plurality of loaded bits based upon the recovered clock signal and the decoded address signal into a latch, and

20 generating said plurality of bits from the latch.

1/6

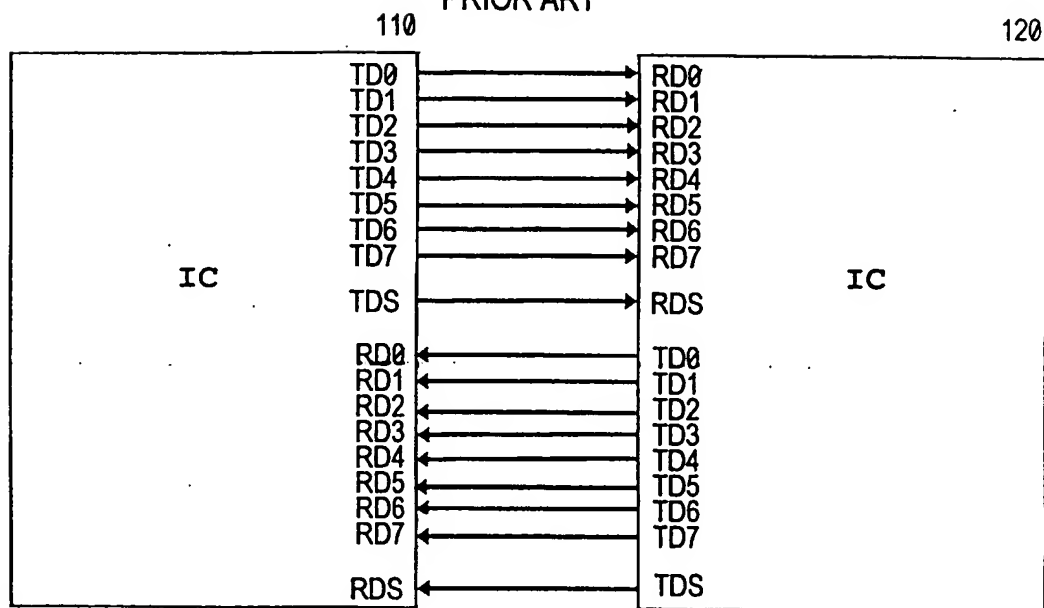
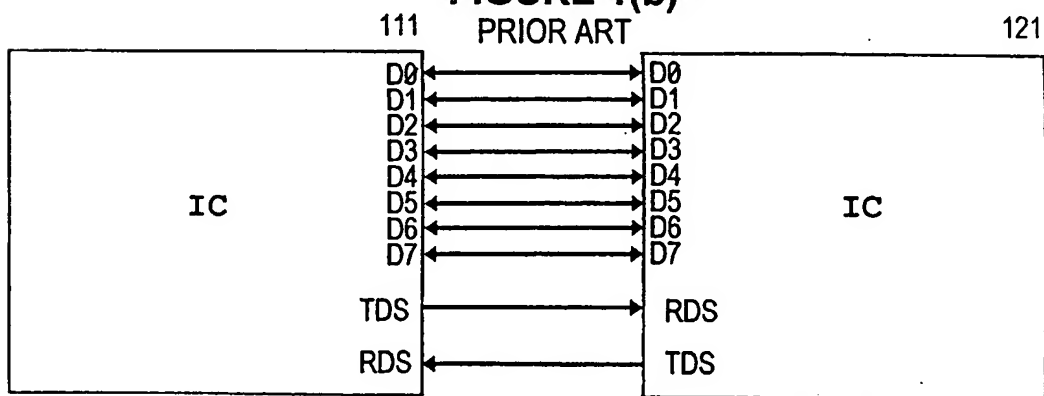
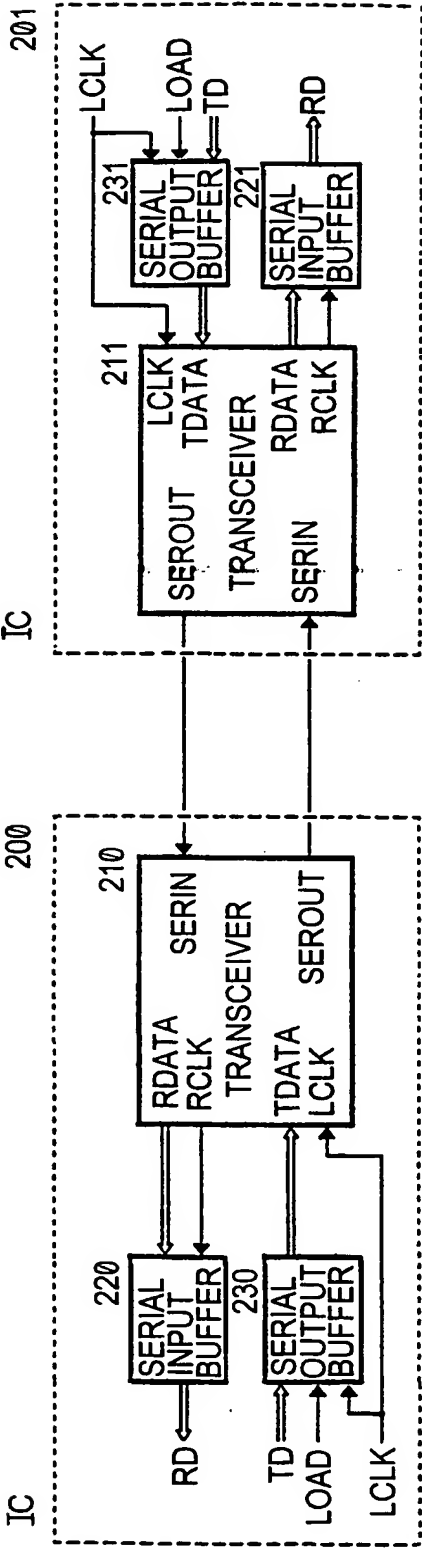
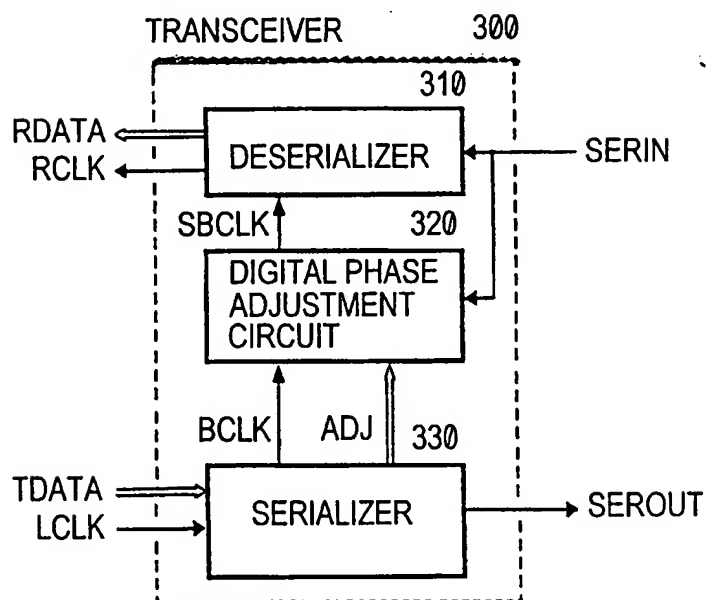
FIGURE 1(a)
PRIOR ART**FIGURE 1(b)**
PRIOR ART

FIGURE 2



3/6

FIGURE 3(a)

4/6

FIGURE 3(b)

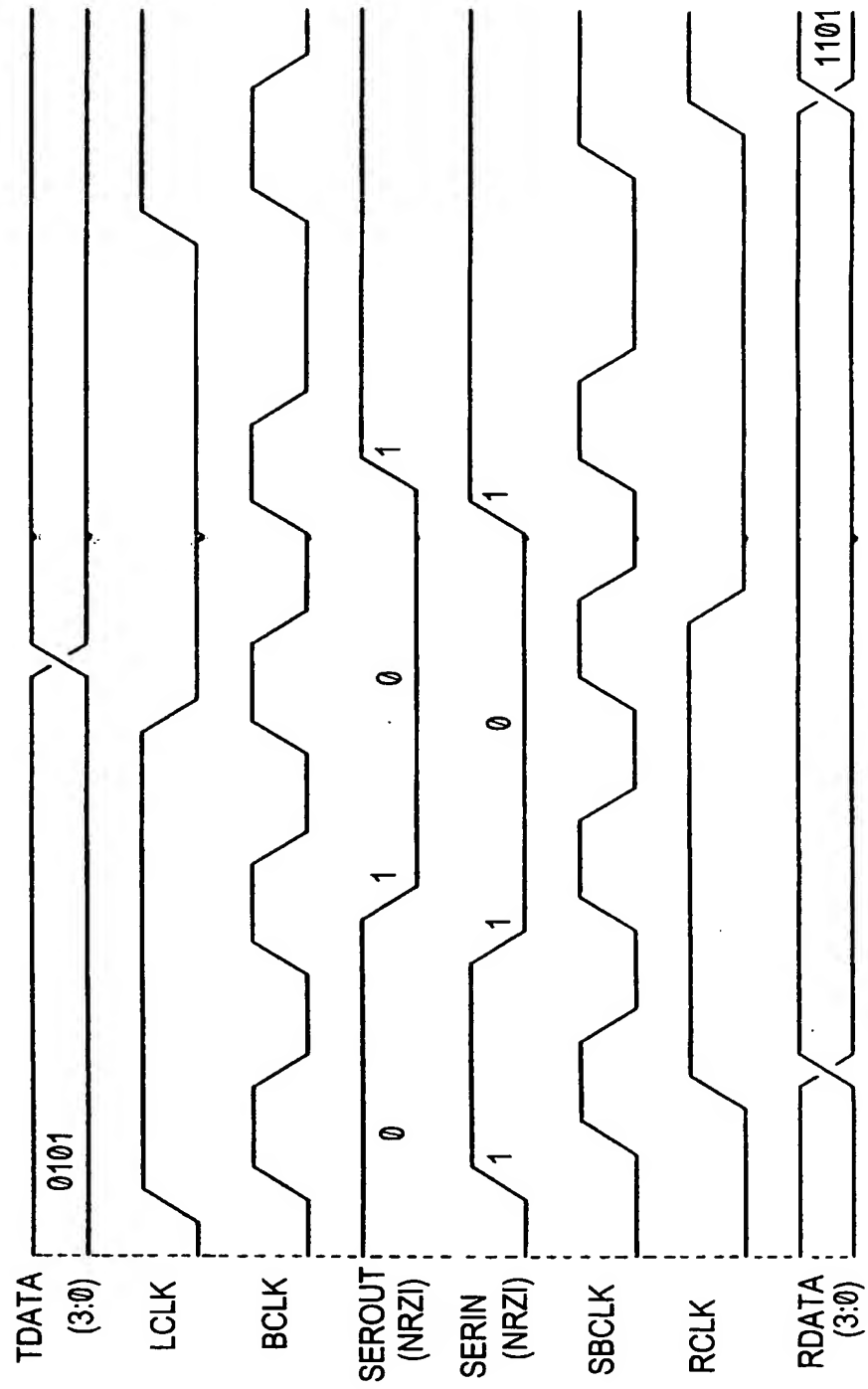


FIGURE 4(a)

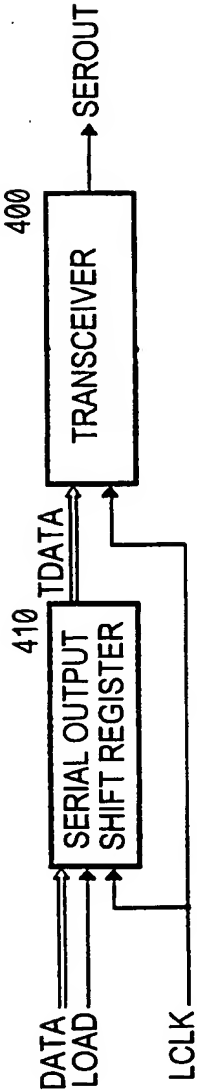
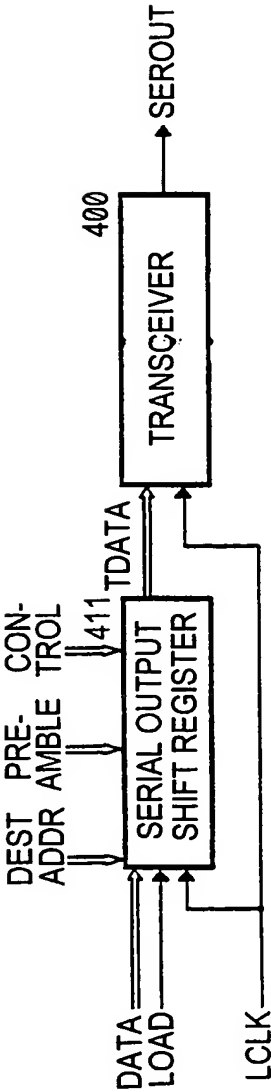


FIGURE 4(b)



6/6

FIGURE 5(a)

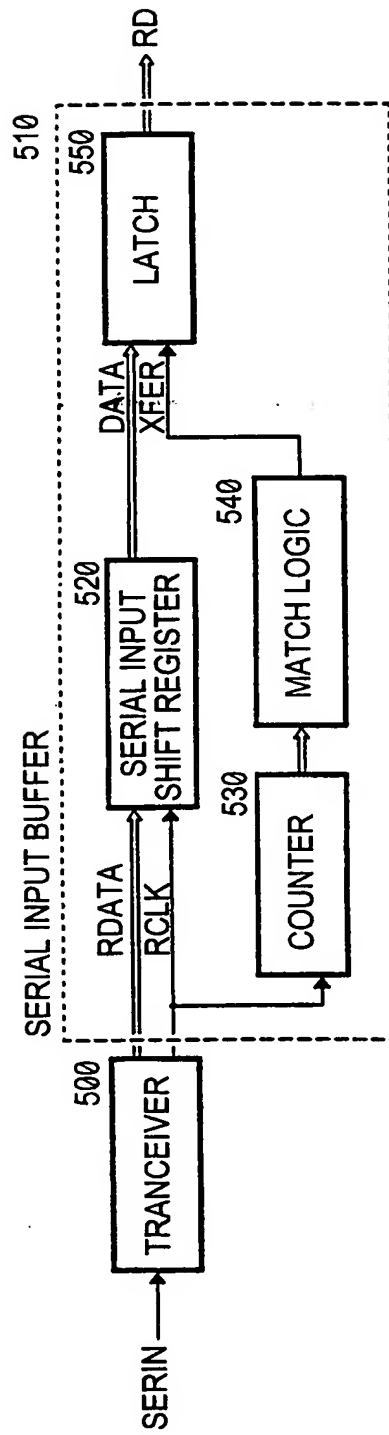
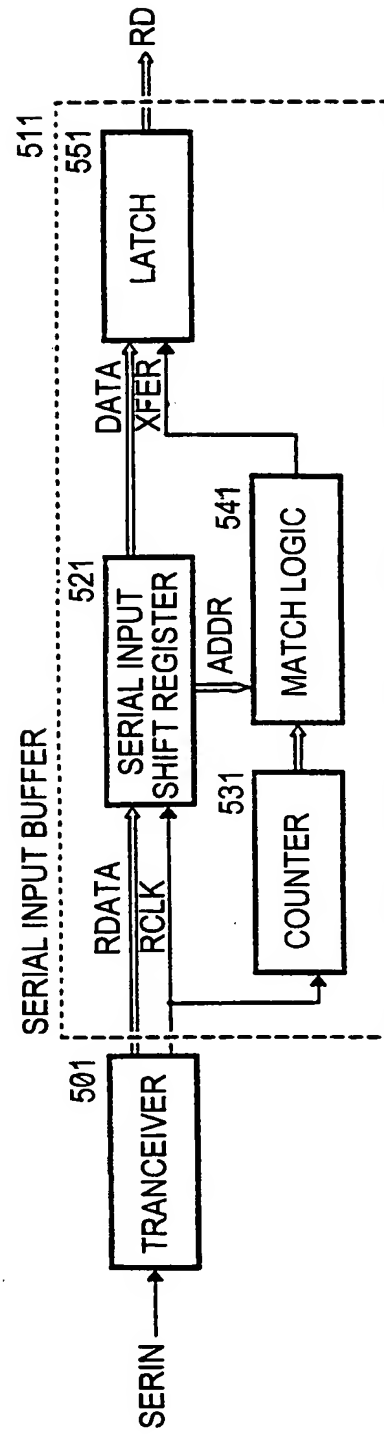


FIGURE 5(b)



INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 97/21936

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F13/42 G11C5/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G06F G11C H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 744 752 A (AT & T CORP) 27 November 1996	1-3, 7, 8
Y	see column 4, line 44 - column 7, line 54; figures 2, 3	4-6
X	US 5 237 322 A (HEBERLE KLAUS) 17 August 1993	1
Y	see the whole document	4-6
A	US 4 148 099 A (LAUFFER DONALD K ET AL) 3 April 1979 see abstract; figures 1-3	1-8
	-/-	



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

13 March 1998

Date of mailing of the international search report

23/03/1998

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040. Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Segaert, P

INTERNATIONAL SEARCH REPORT

Int. J. Application No.

PCT/US 97/21936

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SORGENFREI J ET AL: "SCHNITTSTELLEN-IC FUR DEN SERIELLEN KFZ-BUS" ELEKTRONIK, vol. 39, no. 10, 11 May 1990, pages 140-143, XP000117042 see the whole document ---	1-8
A	US 4 159 541 A (LAUFFER DONALD K ET AL) 26 June 1979 ---	
A	EP 0 416 714 A (ANAMARTIC LTD) 13 March 1991 ---	
A	EP 0 597 583 A (NOKIA MOBILE PHONES LTD) 18 May 1994 -----	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 97/21936

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0744752 A	27-11-96	US 5696928 A CA 2176988 A JP 9017175 A	09-12-97 23-11-96 17-01-97
US 5237322 A	17-08-93	EP 0489944 A DE 59009700 D US 5495240 A	17-06-92 26-10-95 27-02-96
US 4148099 A	03-04-79	DE 2857457 C EP 0015940 A FR 2423029 A GB 2037520 A,B JP 1435016 C JP 54134935 A JP 62043277 B NL 7902352 A WO 7900912 A	26-07-84 01-10-80 09-11-79 09-07-80 07-04-88 19-10-79 12-09-87 15-10-79 15-11-79
US 4159541 A	26-06-79	DE 2828698 A DE 2828726 A FR 2401490 A FR 2430066 A GB 2000617 A,B GB 2000618 A,B JP 1371955 C JP 54014130 A JP 61041074 B NL 7806802 A,B NL 7806803 A,B	18-01-79 18-01-79 23-03-79 25-01-80 10-01-79 10-01-79 07-04-87 02-02-79 12-09-86 03-01-79 03-01-79
EP 0416714 A	13-03-91	GB 2177825 A DE 3681724 A DE 3683477 A EP 0229144 A EP 0231237 A GB 2178204 A,B WO 8700674 A WO 8700675 A GB 2207785 A,B JP 63500545 T	28-01-87 31-10-91 27-02-92 22-07-87 12-08-87 04-02-87 29-01-87 29-01-87 08-02-89 25-02-88

INTERNATIONAL SEARCH REPORT

Information on patent family members

In .tional Application No

PCT/US 97/21936

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0416714 A		JP 63500618 T US 5072424 A US 4943946 A	03-03-88 10-12-91 24-07-90
EP 0597583 A	18-05-94	FI 924588 A JP 6282523 A US 5446772 A	10-04-94 07-10-94 29-08-95